

# **SUBSTRATE ENGINEERING FOR OPTIMUM CMOS DEVICE PERFORMANCE**

## **Abstract**

An integrated semiconductor structure having different types of complementary metal oxide semiconductor devices (CMOS), i.e., PFETs and NFETs, located atop a semiconductor substrate, wherein each CMOS device is fabricated such that the current flow for each device is optimal is provided. Specifically, the structure includes a semiconductor substrate that has a (110) surface orientation and a notch pointing in a  $\langle 001 \rangle$  direction of current flow; and at least one PFET and at least one NFET located on the semiconductor substrate. The at least one PFET has a current flow in a  $\langle 110 \rangle$  direction and the at least one NFET has a current flow in a  $\langle 100 \rangle$  direction. The  $\langle 110 \rangle$  direction is perpendicular to the  $\langle 100 \rangle$  direction. A method of fabricating such as integrated semiconductor structure is also provided.